***pray for your life if this comes up on the exam └༼ ಥ ᗜ ಥ ༽┘( ͠° ͟ʖ ͡°)***

***ᕙ༼ຈل͜ຈ༽ᕗ flex your barryBot ᕙ༼ຈل͜ຈ༽ᕗ***

**Low-power design**

Design for maximising battery life. Increase power-efficiency to give:

* better performance
* more CPU cycles for compression, ECC
* reduce radio power
* longer battery life

Lower power gives market advantage.

**CMOS (a technology for constructing integrated circuits)**

* voltage change on a gate requires charge transfer, and therefore power consumption
* once a gate is charged it can maintain its level without any additional charge movement

CMOS circuitry **only** consumes power when switching states (unless leakage)

//Then diagrams appear I don’t understand//

**Dynamic Power Consumption**

simplified to:

= total node capacitance

= switching frequency of device clock

= supply voltage

= mean overall activity = mean number of transitions per clock cycle = 2 for gates connected to a clock

**and more equations… see lecture**

**Energy consumption:**

If P(Power) is constant, Energy = P \* Time (in Joules).

In battery powered mobile devices, we must worry about both P and E.

If P is too high, overheating may occur.

If P is reduced, but computing time is too high, battery life will be affected.

**Chip design**

Mobile systems are complex SoCs.

All functions (except for maybe large memories) are on a single chip.

Interconnected using bus architectures, built using automated design tools.

Based around reusable “IP Blocks”, proprietary or brought in (eg ARM processor cores)

Principles of low-power design

* Minimise activity - but most consider trade offs with compression, ECC, RF power
* Localise the activity
  + use on-chip rather than off-chip memory
  + use cache to minimise access to large off-chip memory
  + plan streaming data movement to minimise bandwidth and distance moved